Claims 1, 28 and 34 are rejected under 35 U.S.C. 102(e) as being anticipated by Akimoto et al. (Patent No.: US 6,756,962).

Response:

Claim 1

As disclosed by Akimoto, the function of the offset canceling buffer outputting switch 16 is integrated into the differential amplifier 26, where the differential amplifier 26 includes a differential stage having transistors 31-39, an amplification stage having transistors 40-42, a source follower stage having transistors 44, 45, and selector switches 55, 56 (Fig. 9, col. 11, lines 7-31). As shown in Fig. 9, the selector switches 55, 56 control the gates of the transistors 44, 45 that determine when they are connected to ground. That is, the on/off status of the selector switches 55, 56 determines on/off status of the transistors 44, 45. As recited in col. 11, lines 33-38, the transistors 44, 45 are turned off if their gates are provided with ground voltages due to the selector switches 55, 56 being turned on, and the differential amplifier 26 drives the signal line if the selector switches 55, 56 are turned off to make the transistors 44, 45 activated. Therefore, the transistors 31-42 in the differential stage and the amplification stage are always operating since gate voltages of the transistors 31-42 are not controlled by the selector switches 55, 56. In other words, if the selector switches 55, 56 are turned on, the transistors 31-42 are still activated to process the received driving voltage level for the corresponding pixel, but transistors 44, 45 are inactivated to stop the processed driving voltage level from being outputted to drive the corresponding pixel; in addition, if the selector switches 55, 56 are turned off, the transistors 31-42 are still activated to process the received

driving voltage level for the corresponding pixel, and the transistors 44, 45 are activated to output the processed driving voltage level to drive the corresponding pixel. Throughout the entire specification, Akimoto does not teach or suggest any technique related to saving power consumed by the differential amplifier 26 by stopping the differential amplifier 26 from processing the received driving voltage level for the pixel. In short, Akimoto fails to teach or suggest the claimed feature "**turning off the operating voltages inputted into the corresponding output buffers for stopping the output buffers from processing the corresponding driving voltage levels.**"

Applicants believe that the rejection under 35 U.S.C. 102(e) is overcome, and the amended claim 1 has been placed in condition for allowance. Reconsideration of the amended claim 1 is respectfully requested. Claims 3-20 are dependent on amended claim 1, and should be allowed if amended claim 1 is found allowable.

Claim 28

For the same reason stated under **Claim 1** above, applicants believe that rejection under 35 U.S.C. 102(e) is overcome, and the claim 28 has been placed in condition for allowance. Reconsideration of claim 28 is respectfully requested.

Claim 34

According to Akimoto's teachings, odd-number rows and even-number rows of the signal lines 7 are alternately connected to the upper write circuit and the lower write circuit by

alternately performing switching of connection of the signal lines 7 to the offset canceling buffer outputting switches 66 and the signal line shunting switches 67 for each field (Fig. 11, col. 12, lines 36-43). Therefore, as shown in Fig. 9, it is obvious that a **single** switch 67 is unable to connect two pixels at the same time. That is, the single switch 67 is either connected to a pixel disposed at an odd-number row or a pixel disposed at an even-number row, and is **unable to establish a connection linking two pixels.** Therefore, Akimoto fails to teach or suggest the claimed feature "each second switch connected between corresponding two pixels for selectively **connecting the corresponding two pixels.**"

Applicants believe that rejection under 35 U.S.C. 102(e) is overcome, and the claim 34 has been placed in condition for allowance. Reconsideration of claim 34 is respectfully requested.

Claims 29 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akimoto et al. (Patent No.: US 6,756,962).

Response:

Claim 29

As stated by examiner, it would be obvious to obtain each of the second switches connected between two pixels by turning on a switch of the upper circuit for an odd pixel and turning on a switch of the lower circuit for an even pixel. However, applicants deem that Akimoto's disclosure has been misinterpreted. For the same reason stated under **Claim 34** above, the

switch 67 taught by Akimoto is unable to connect two pixels at the same time. That is, the single switch 67 is either connected to a pixel disposed at an odd-number row or a pixel disposed at an even-number row, and is **unable to establish a connection linking two pixels.** Akimoto fails to teach or suggest the claimed feature "a second switch connected between the output terminal of said driving unit and an output terminal of another driving unit, **the output terminal of said driving unit being electrically connected to the output terminal of another driving unit when said second switch is turned on.**" In short, based on Akimoto's teachings, it is not obvious for a skilled person to obtain each of the second switches connected between two pixels.

Applicants believe that rejection under 35 U.S.C. 103(a) is overcome, and the claim 29 has been placed in condition for allowance. Reconsideration of claim 29 is respectfully requested.

Claim 39

For the same reason stated under Claim 29 above, Akimoto fails to teach or suggest the claimed feature "a plurality of second switch circuits each coupled between two pixels for selectively connecting the two pixels." In short, based on Akimoto's teachings, it is not obvious for a skilled person to obtain each of the second switches connected between two pixels.

Applicants believe that rejection under 35 U.S.C. 103(a) is overcome, and the claim 39 has been placed in condition for allowance. Reconsideration of claim 39 is respectfully

requested.

Claims 21, 35 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akimoto et al. (Patent No.: US 6,756,962) in view of Shimizu (Pub No. US2004/019212).

Response:

Claim 21

According to Shimizu's teachings, a frequency divider is used for generating a reference frequency by dividing an output from a clock generation source 11 by N (Fig. 2, paragraph [0044]). The following components: phase comparator 14A, loop filter 15A, and VCO 16A, are all utilized to lock the desired output F when phases of outputs of the frequency dividers 12 and 13A match (paragraph [0045]). As stated by the examiner, the frequency divider 12 serves as a counter for counting the divided clock signal generated from the frequency divider 12. However, Shimizu's disclosure is misinterpreted. The output of the frequency divider 12, frequency-divided clock, is passed to the phase comparator 14A for phase comparing. Shimizu does not teach utilizing the frequency divider 12 to count the divided clock generated from the frequency divider 12. In other words, Shimizu does not teach or suggest feeding the output of the frequency divider 12 into the frequency divider 12. Shimizu discloses using a programmable counter to implemented the frequency divider 12 (paragraph [0044]); however, as is known to those skilled in this art, the programmable counter is for counting clock cycles of the incoming reference clock f instead of the output (i.e., divided clock) of the programmable counter for dividing frequency of the incoming reference clock f. Therefore, Shimizu fails to

teach or suggest the claimed feature "a counter for **counting the divided clock signal** to generate a count value." Since Shimizu fails to teach or suggest counting the divided clock signal to generate a count value, the claimed feature "a comparator for comparing **the count value** with a predetermined number" is new to Shimizu's teachings.

Applicants believe that rejection under 35 U.S.C. 103(a) in view of Akimoto and Shimizu's teachings is overcome, and the claim 21 has been placed in condition for allowance. Reconsideration of the claim 21 is respectfully requested. Claims 22-26 are dependent on claim 21, and should be allowed if claim 21 is found allowable.

Claim 35

For the same reasons as stated under **Claim 21** above, applicants believe that rejection under 35 U.S.C. 103(a) in view of Akimoto and Shimizu's teachings is overcome, and that claim 35 has been placed in condition for allowance. Reconsideration of claim 35 is respectfully requested.

Claim 37

For the same reasons as stated under **Claim 21** above, applicants believe that rejection under 35 U.S.C. 103(a) in view of Akimoto and Shimizu's teachings is overcome, and the claim 37 has been placed in condition for allowance. Reconsideration of claim 37 is respectfully requested.

3. Patentablity of New claims

Claim 40

As stated by examiner, claims 18 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Applicants believe that the new claim 40 has been placed in condition for allowance. Consideration of the new claim 40 is respectfully requested.

Claim 41

As stated by the examiner, claims 24 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Applicants believe that the new claim 41 has been placed in condition for allowance. Consideration of the new claim 41 is respectfully requested.

Applicants respectfully request that a timely Notice of Allowance be issued in this case.

Appl. No. 10/065,665
Amdt. dated Oct. 05, 2005
Reply to Office action of July 12, 2005

Sincerely yours,

Winston Hsu Date: Oct. 05, 2005

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Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 12 hours behind the Taiwan time, i.e. 9 AM in D.C. = 9 PM in Taiwan.)